

FIG.1 (a)

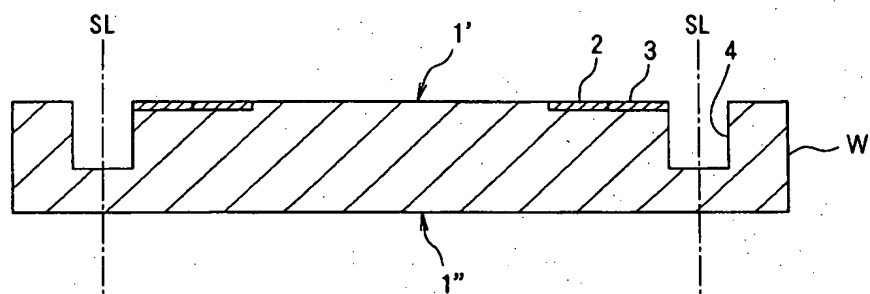


FIG.1 (b)

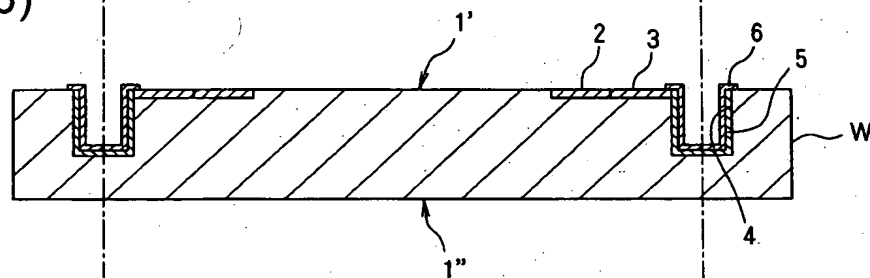


FIG.1 (c)

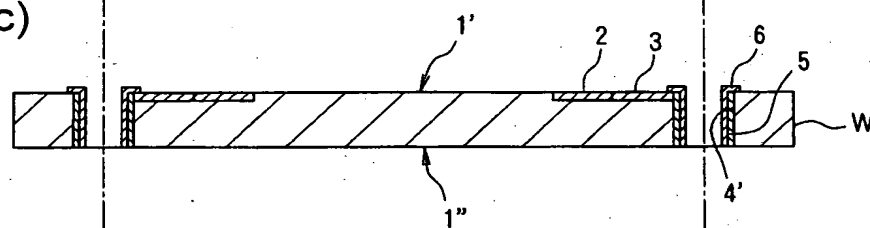


FIG.1 (d)

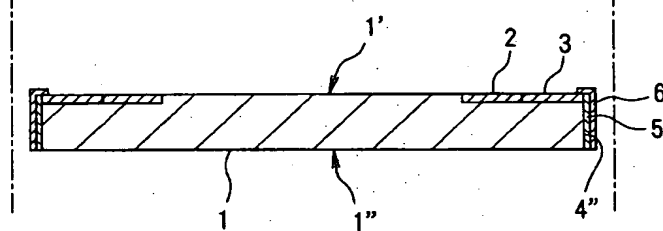


FIG.2 (a)

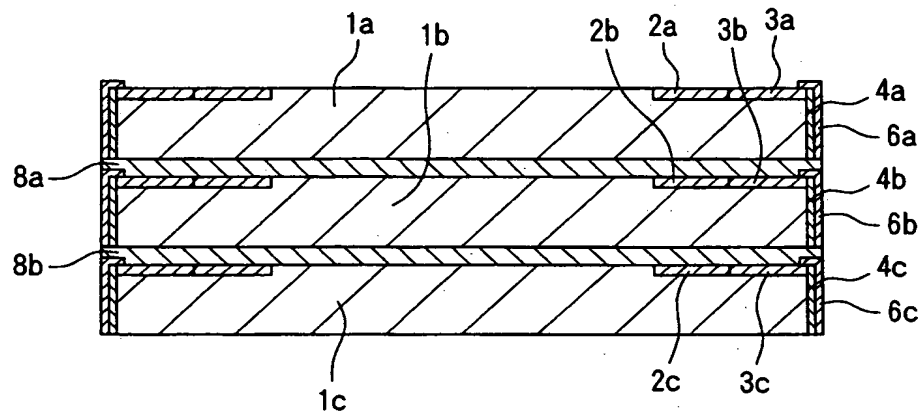


FIG.2 (b)

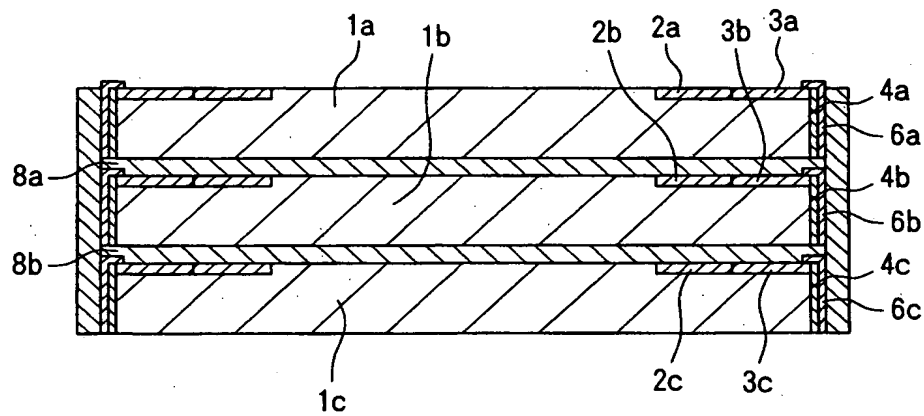


FIG.3 (a)

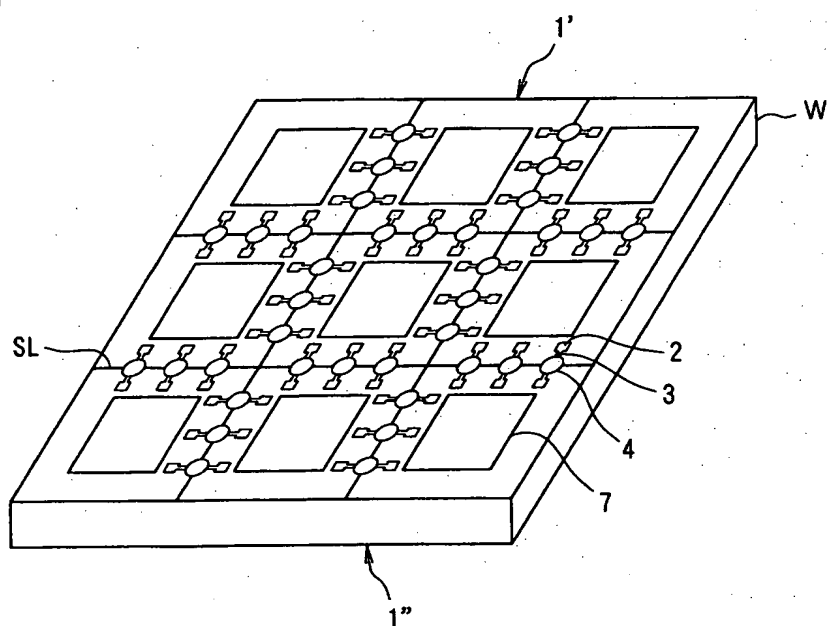


FIG.3 (b)

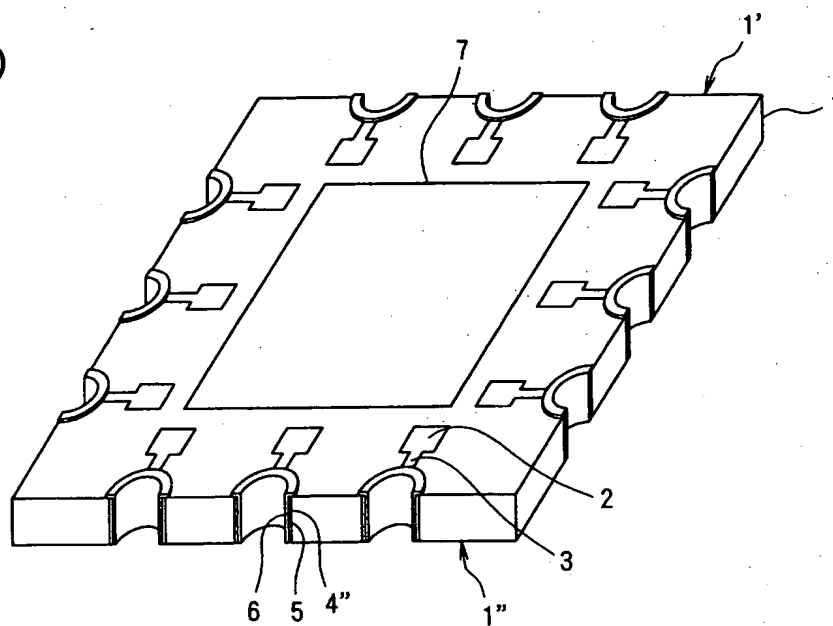


FIG.4 (a)

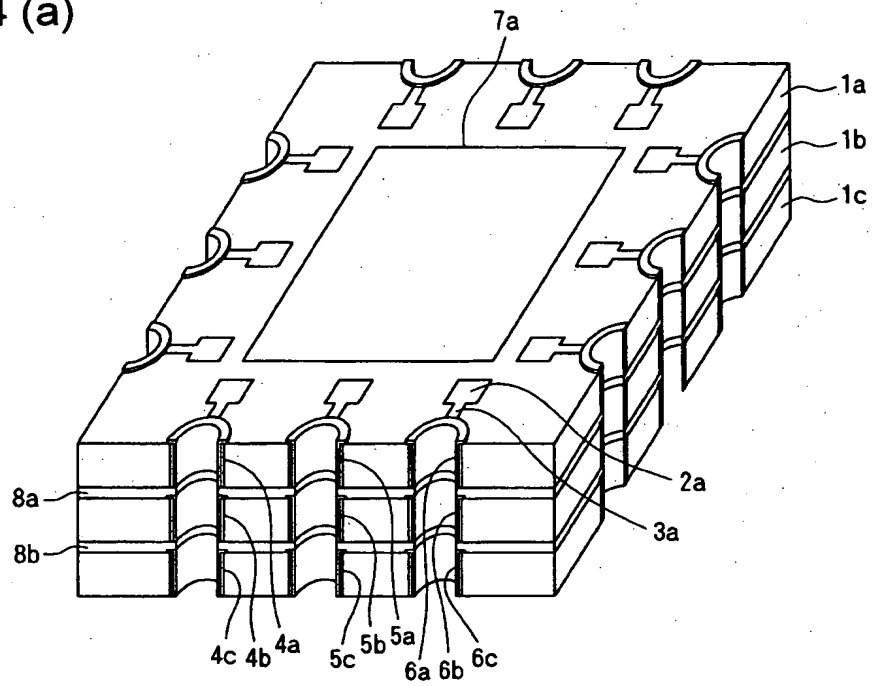


FIG.4 (b)

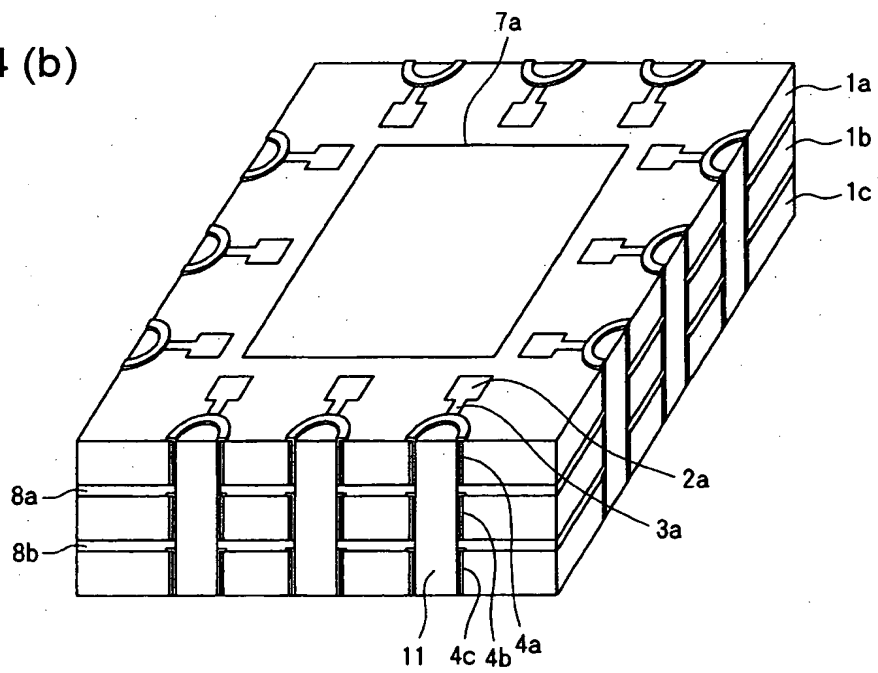


FIG.5 (a)

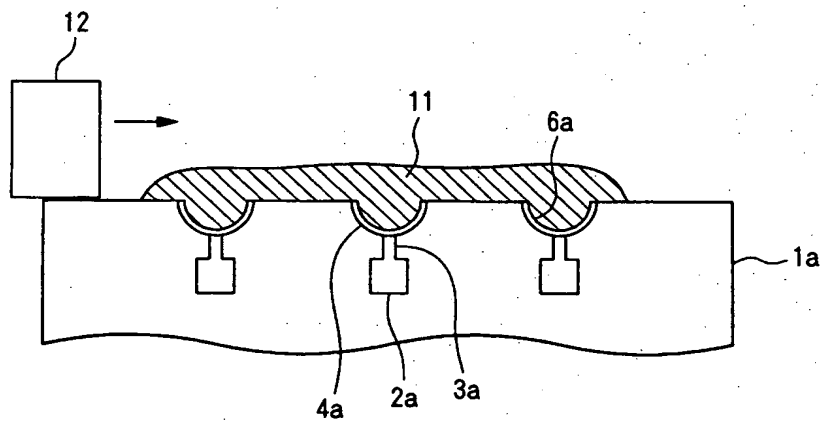


FIG.5 (b)

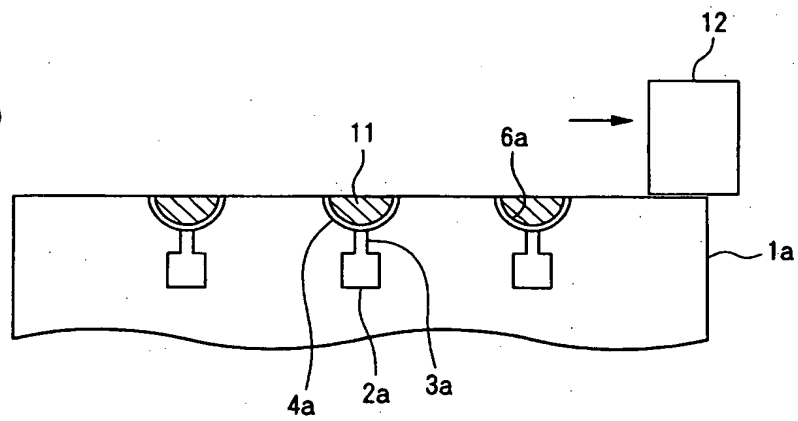


FIG.6 (a)

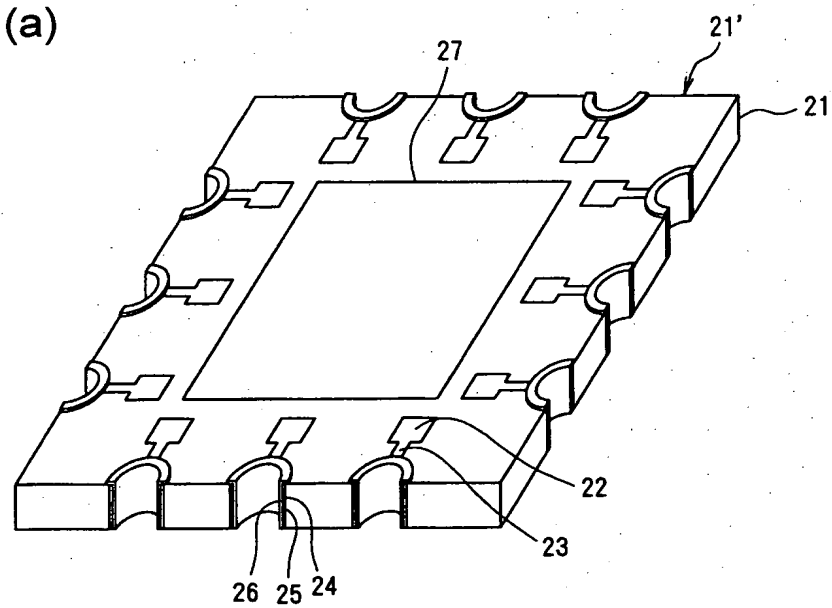


FIG.6 (b)

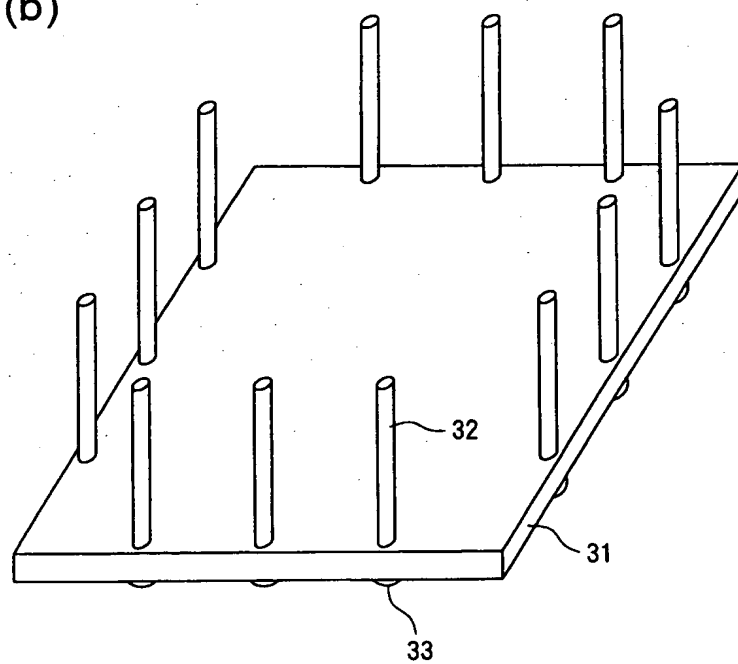


FIG.7 (a)

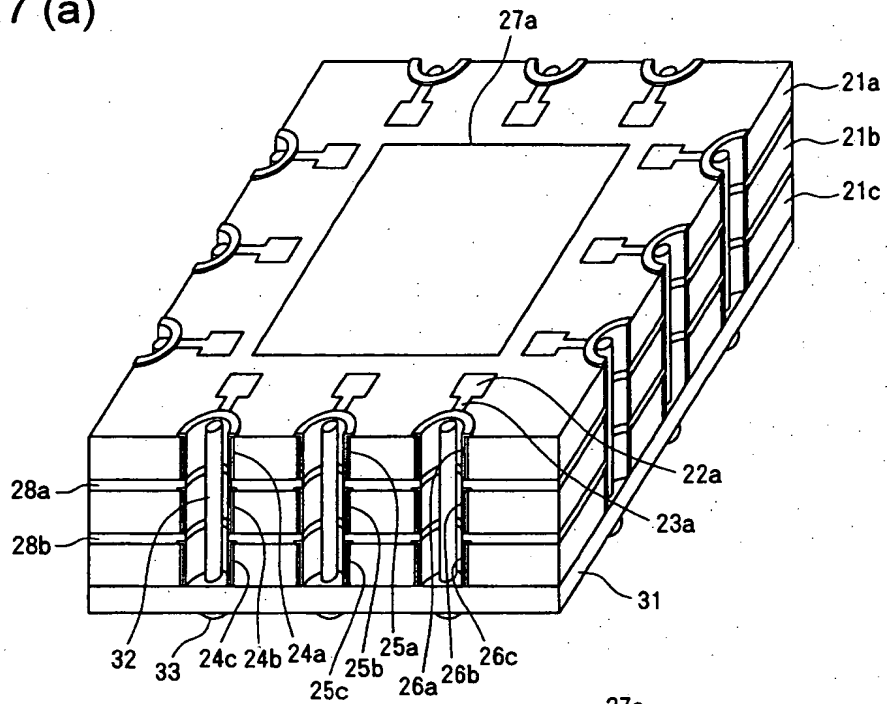


FIG.7 (b)

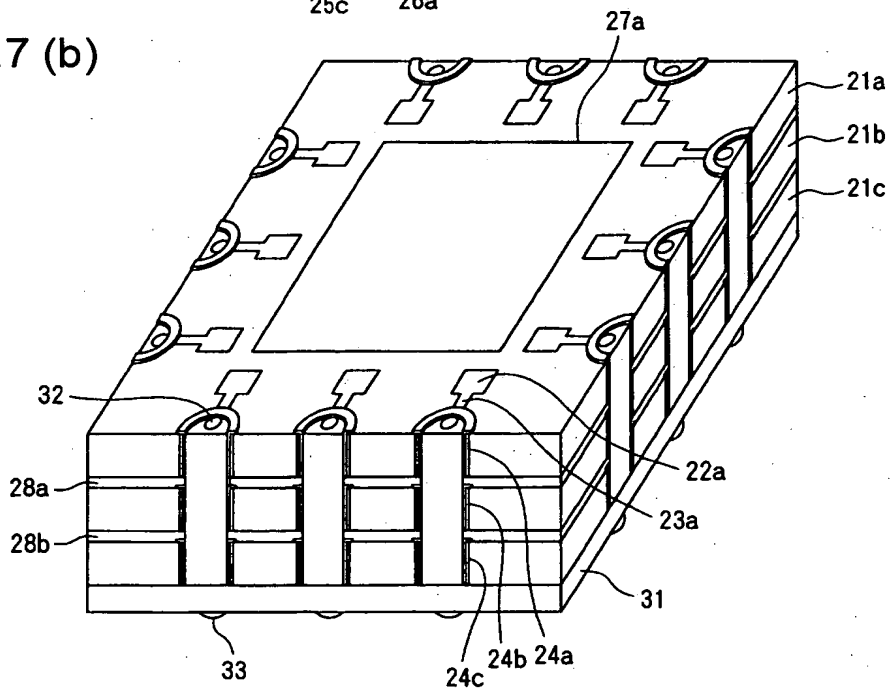


FIG.8

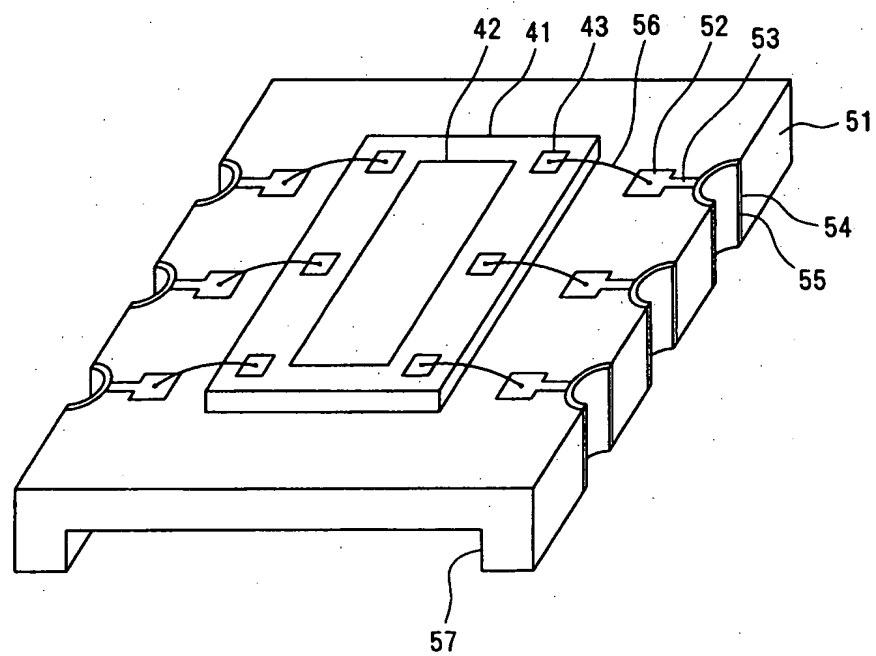




FIG.9 (a)

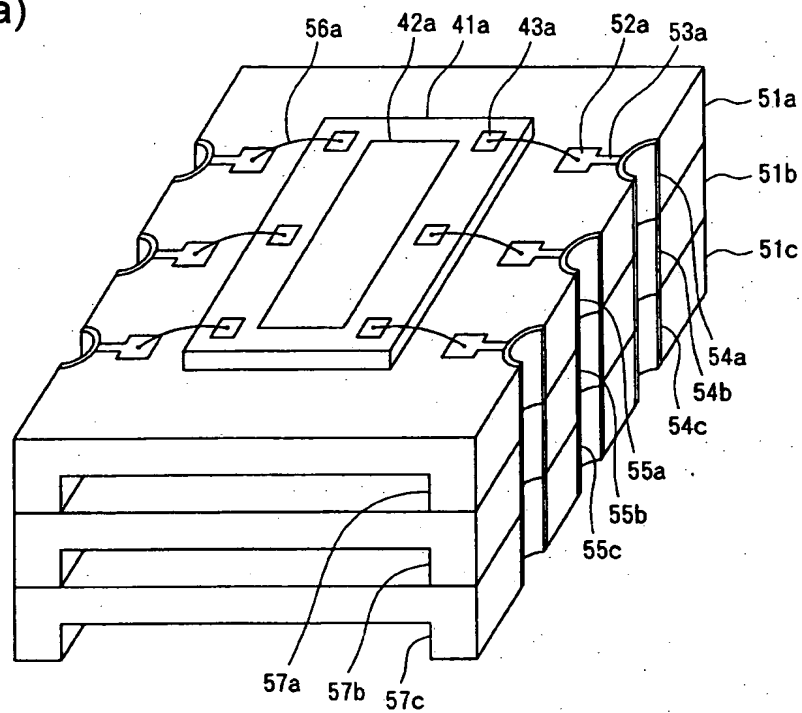


FIG.9 (b)

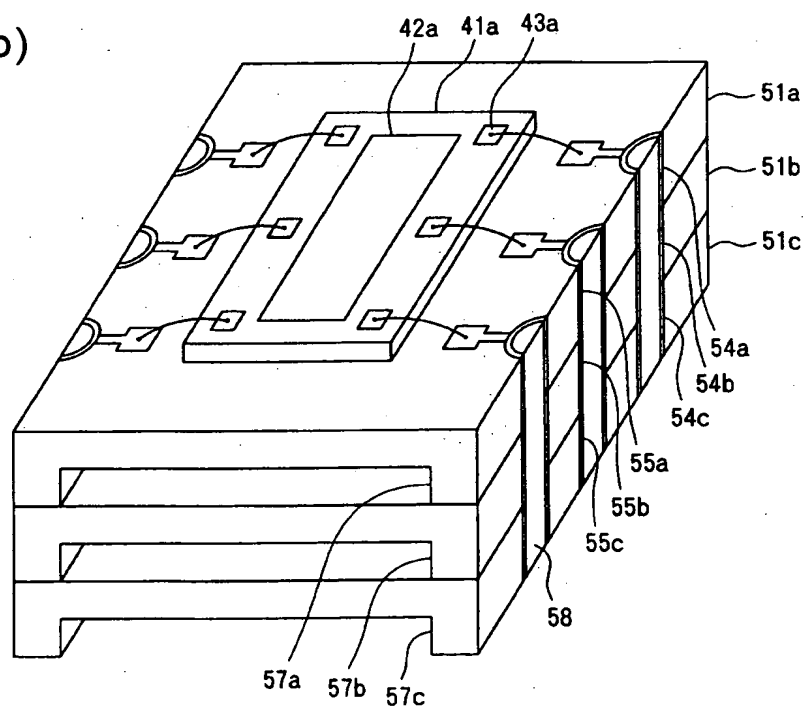


FIG.10 (a)

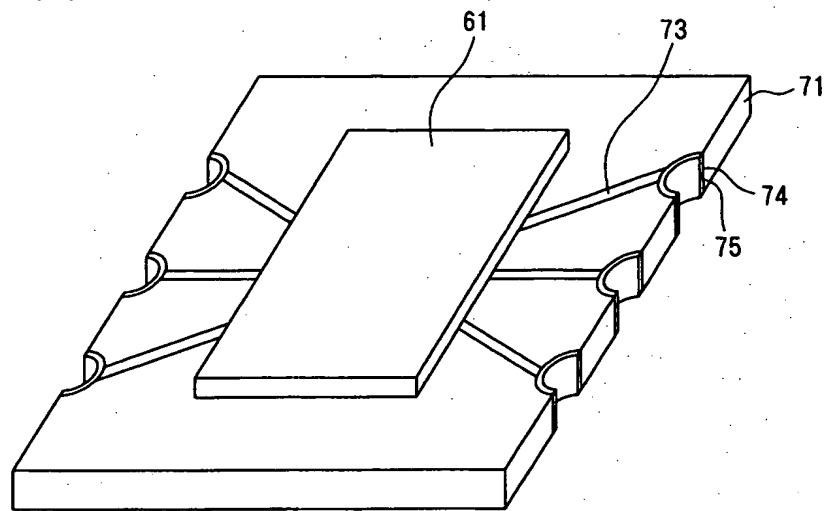


FIG.10 (b)

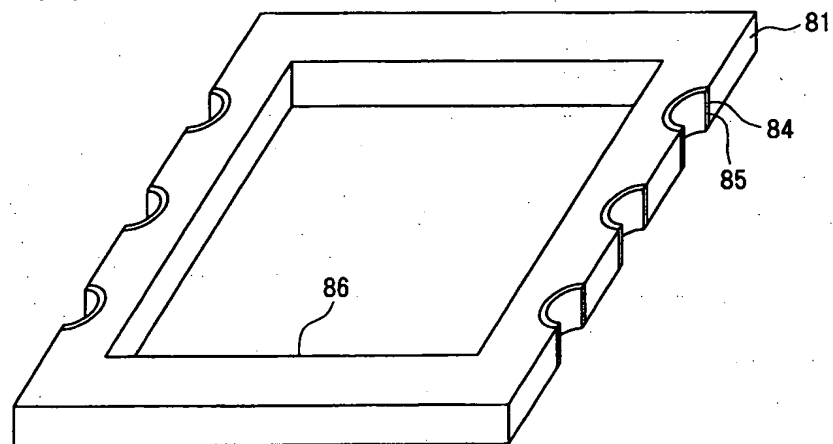


FIG.11 (a)

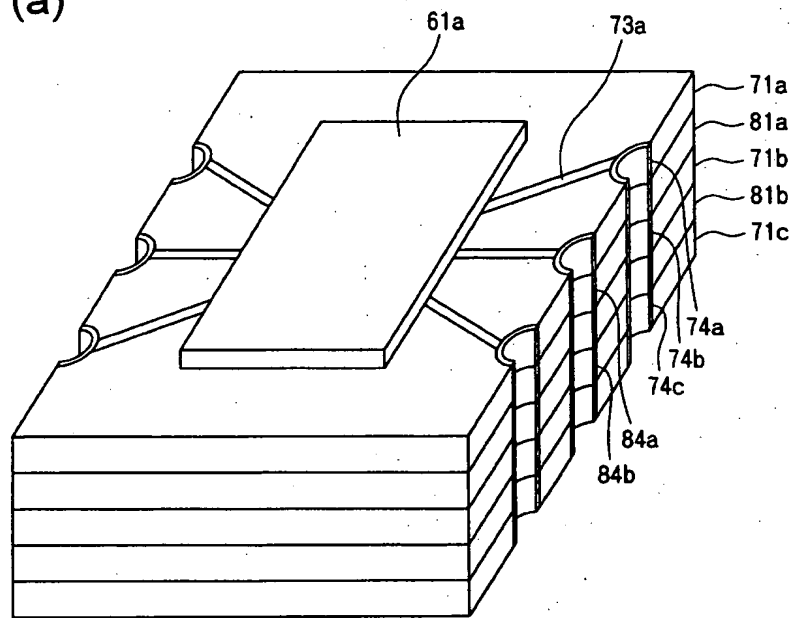


FIG.11 (b)

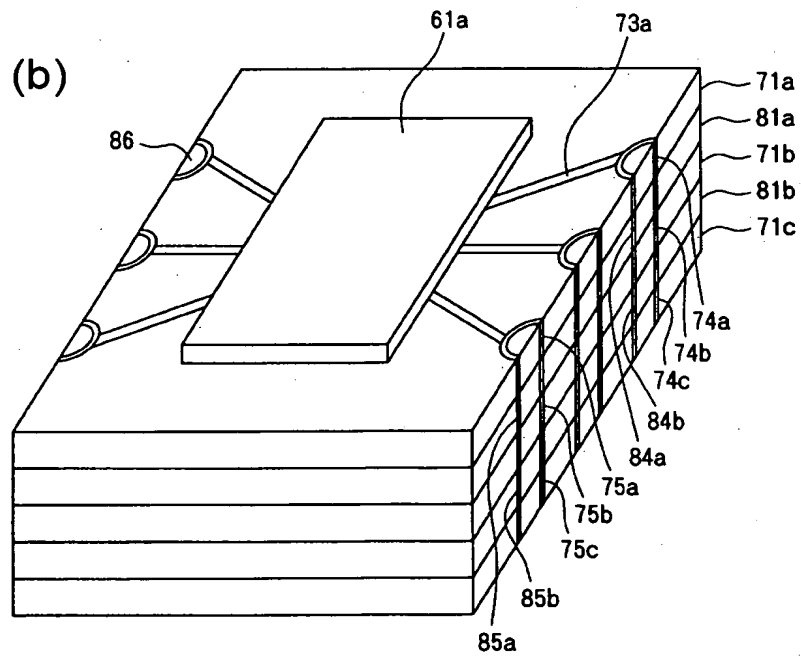


FIG.12 (a)

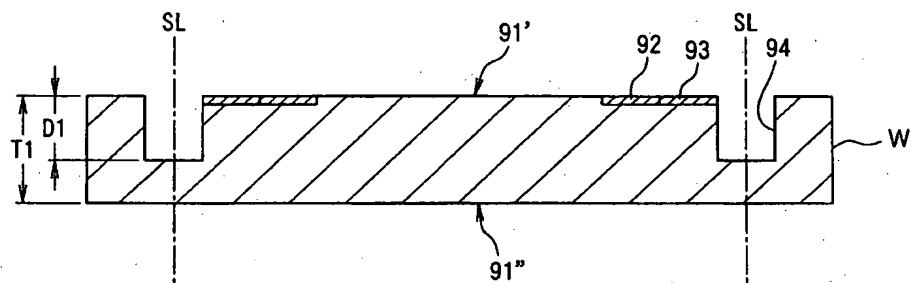


FIG.12 (b)

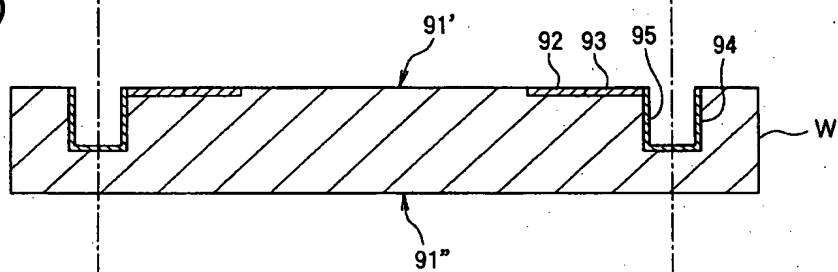


FIG.12 (c)

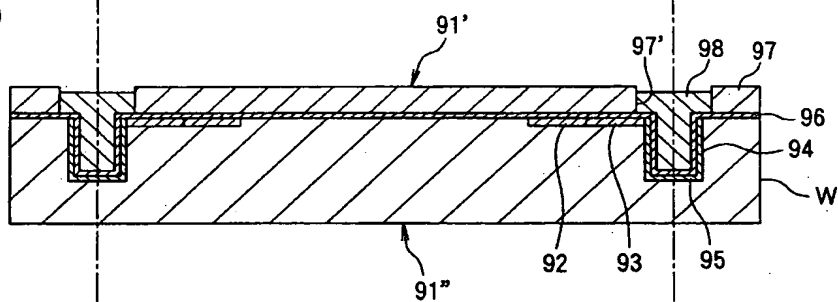


FIG.12 (d)

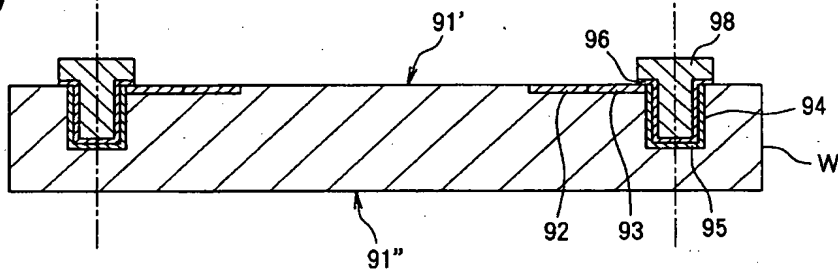


Diagram (b) shows a cross-sectional view of a second embodiment of the semiconductor device. It features a substrate 91'' with a thickness T2. A central layer 91' is formed on the substrate. On the left side, a structure 92 is formed, consisting of a layer 93 and a top layer 94. A side layer 95 is formed on the right side of the central layer 91'. A top layer 96 is formed on the central layer 91'. A side layer 98 is formed on the right side of the central layer 91'. A top layer 99 is formed on the central layer 91'.

FIG.14 (a)  
PRIOR ART

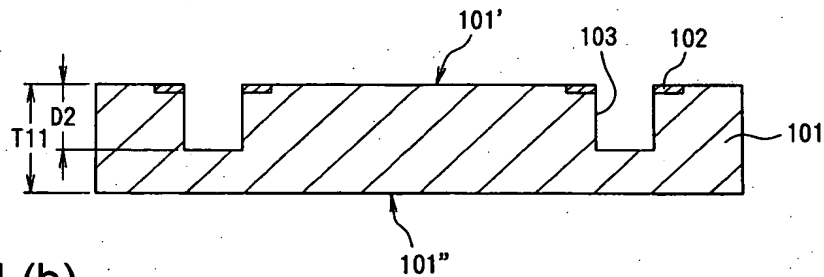


FIG.14 (b)  
PRIOR ART

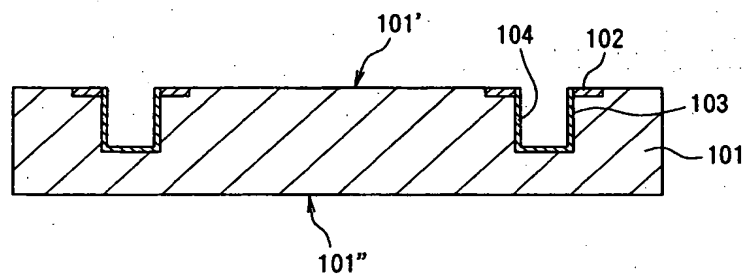


FIG.14 (c)  
PRIOR ART

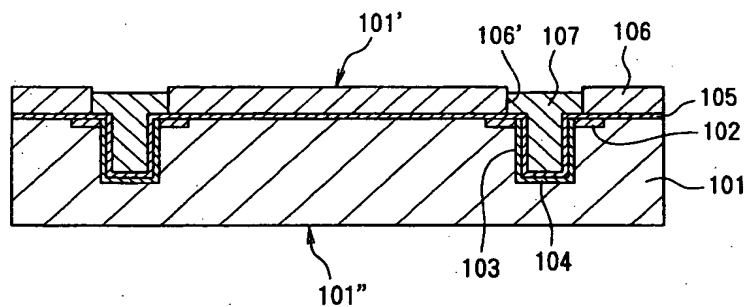


FIG.14 (d)  
PRIOR ART

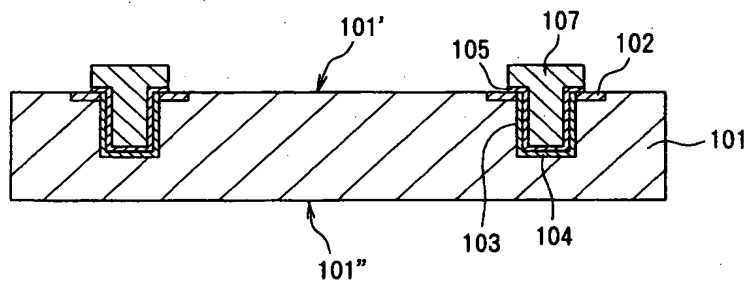


FIG.15 (a)  
PRIOR ART

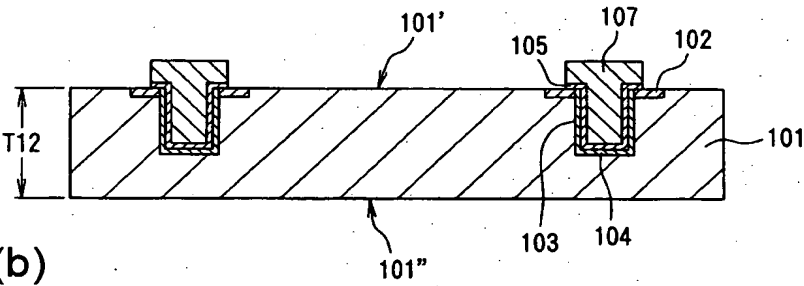


FIG.15 (b)  
PRIOR ART

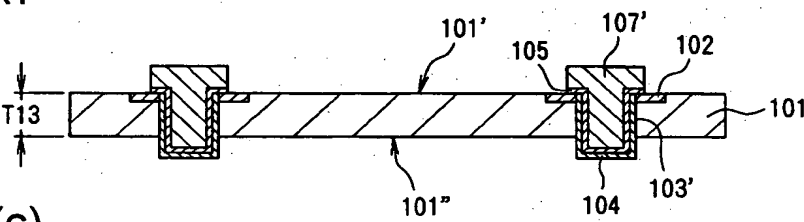


FIG.15 (c)  
PRIOR ART

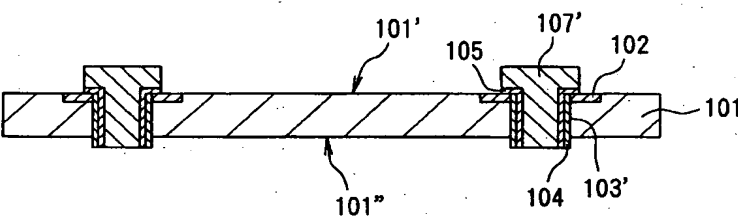


FIG.15 (d)  
PRIOR ART

